

Applicant: Michael Baxter
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' # No.: 20412-02553

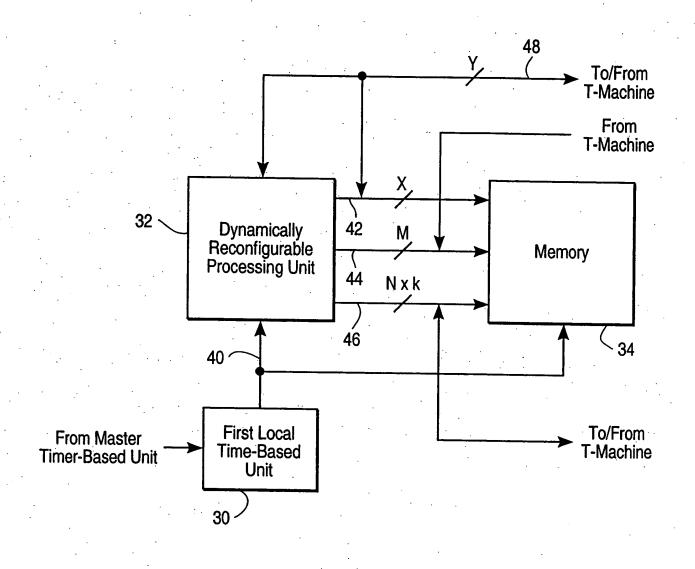


FIG. 2

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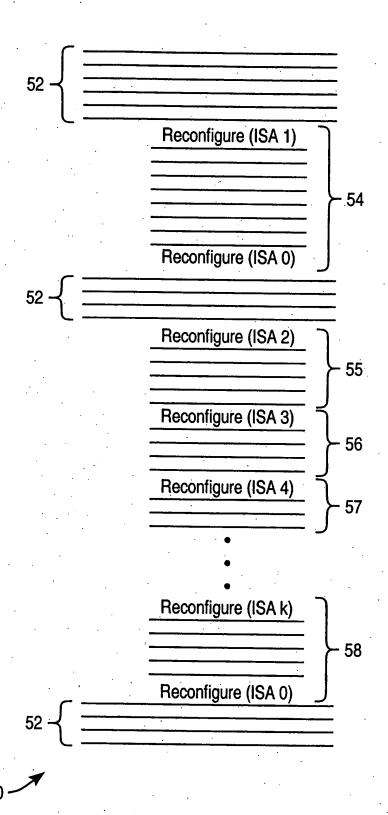
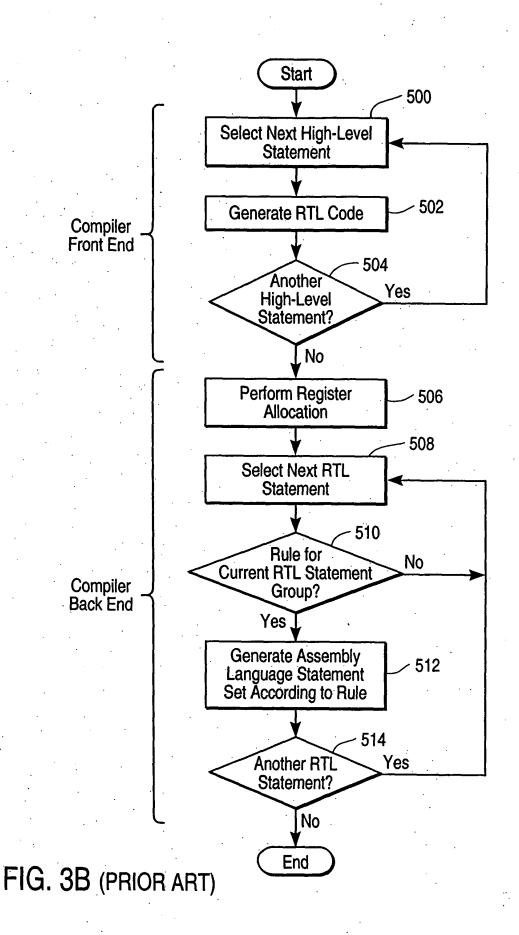


FIG. 3A

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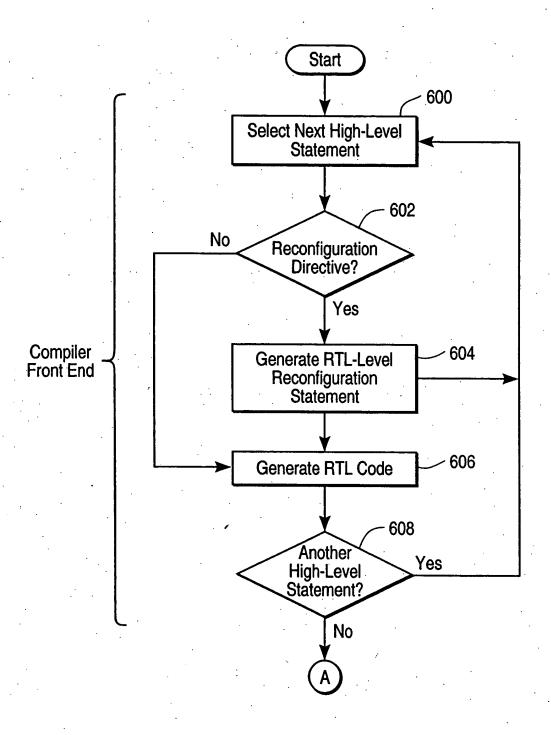


FIG. 3C

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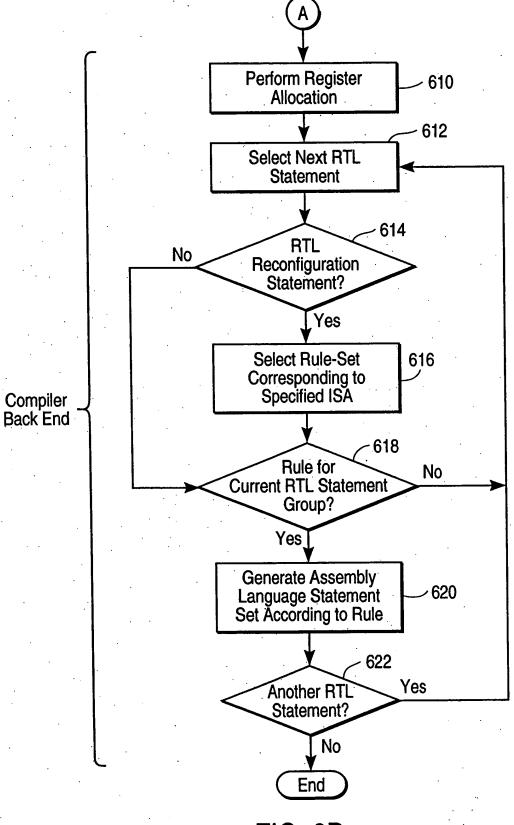
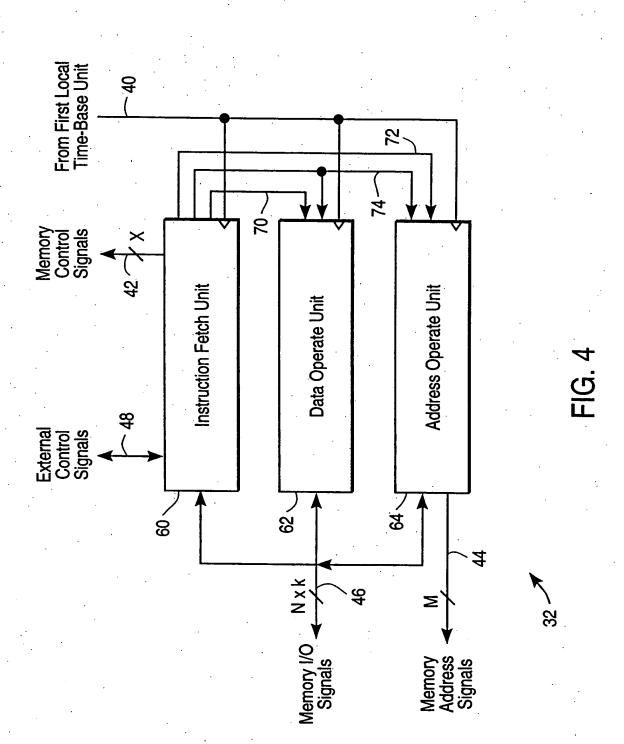


FIG. 3D

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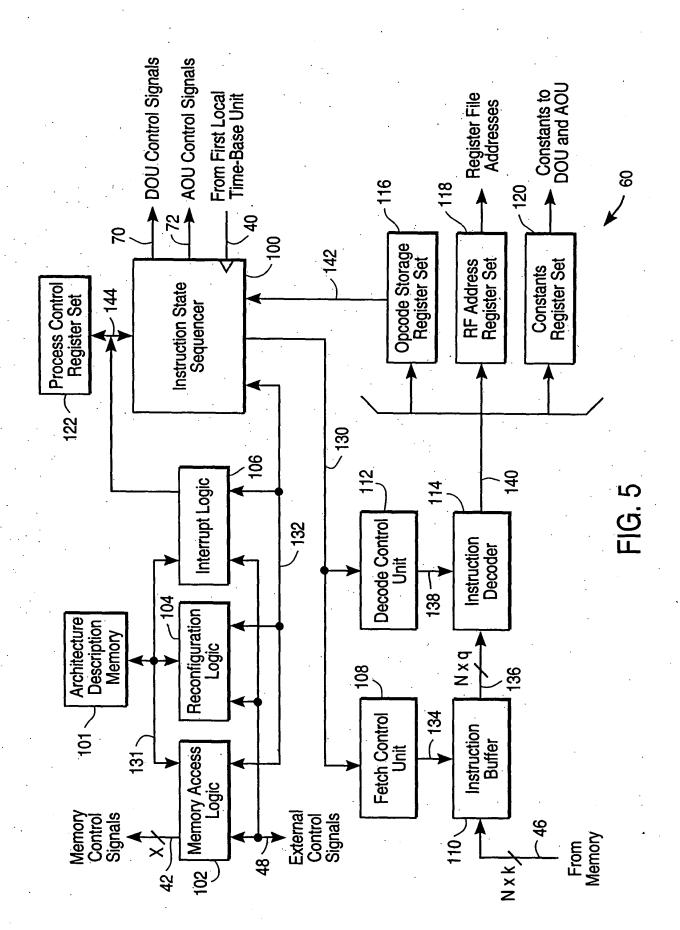
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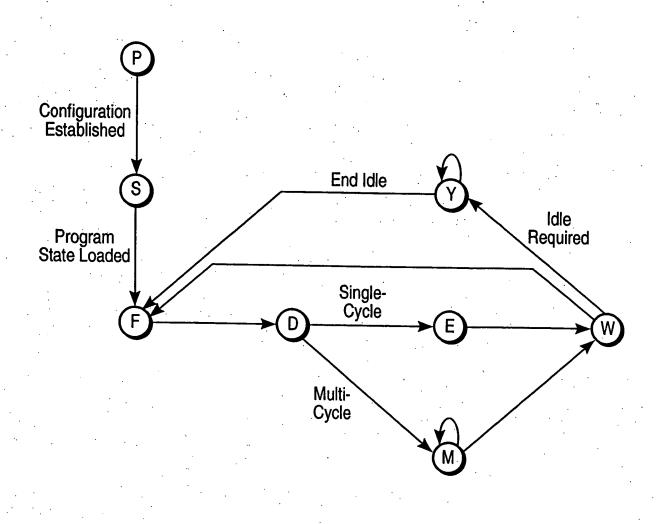
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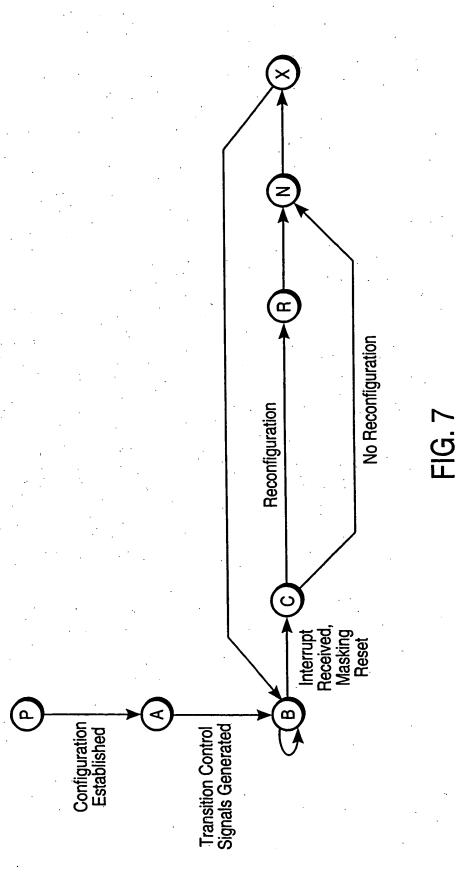
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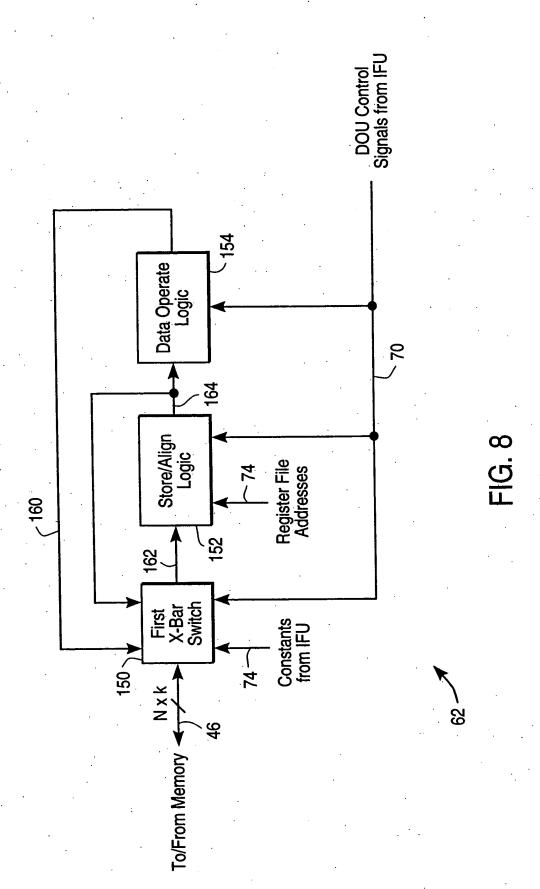
Interrupt Signal Received Interruptable State as Specified by Transition Control Signals Next State as Specified by Transition Control Signals

FIG. 6

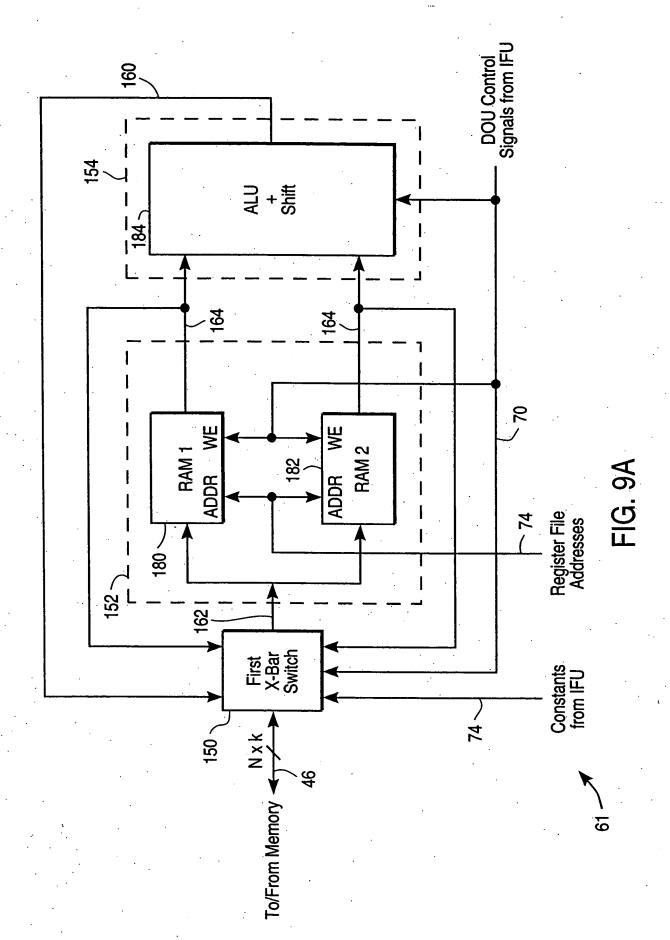
Meta-Address Architecture for Parallel, Dynamically Applicant: Michael Baxter
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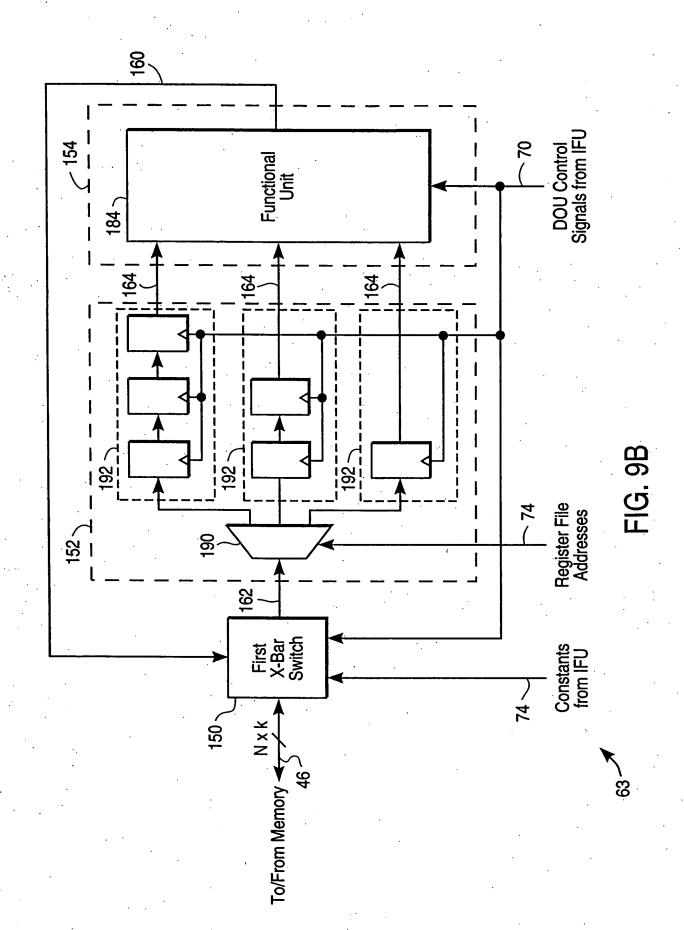
Meta-Address Architecture for Parallel, Dynamically Applicant: Michael Baxter 1ge 11 of 29 S/N 09/255,499 bocket No.: 20412-02553



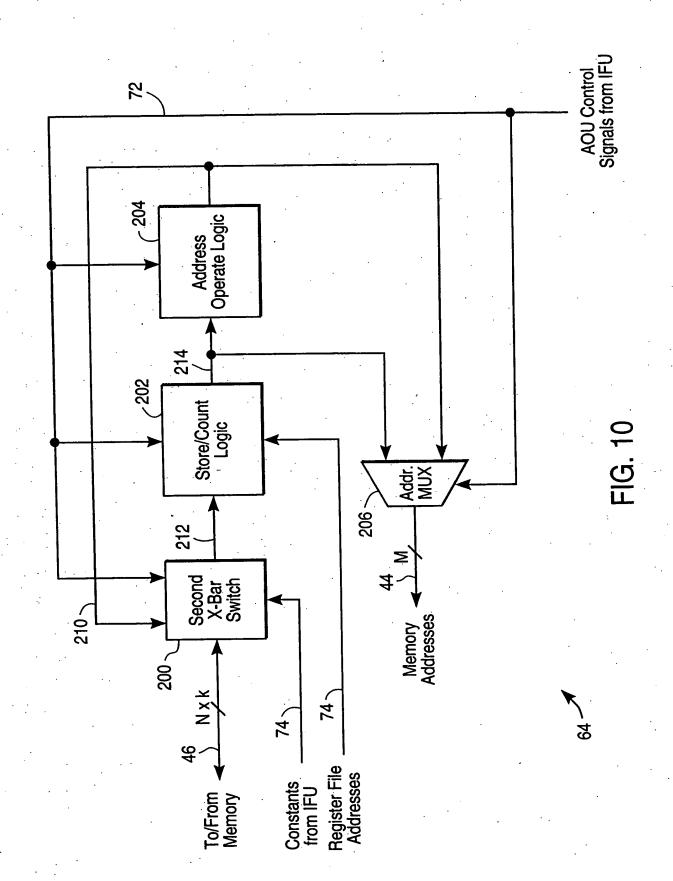
Meta-Address Architecture for Parallel, Dynamically Applicant: Michael Baxter
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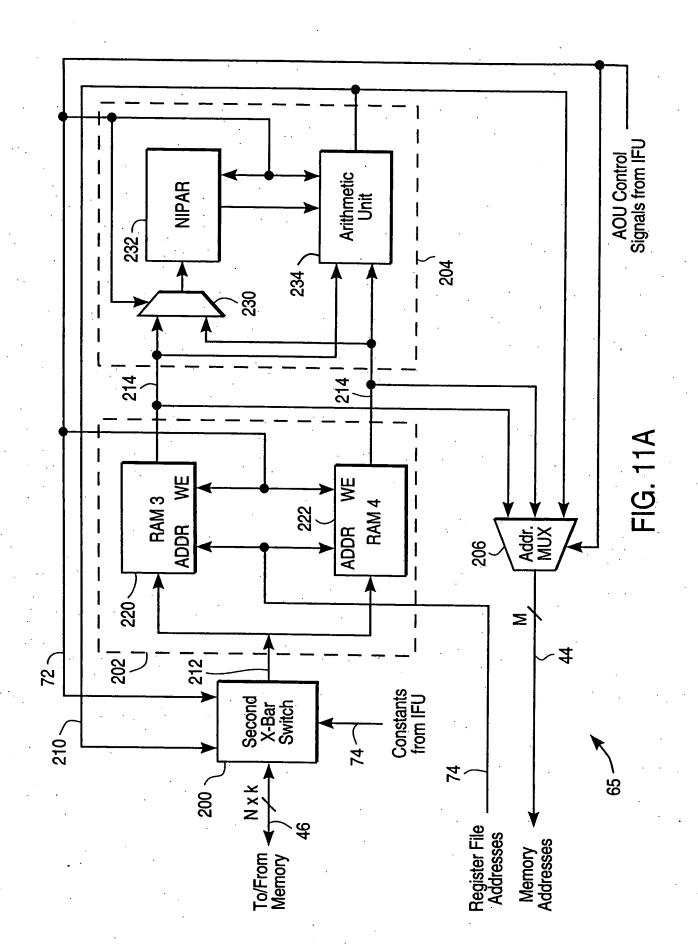
Meta-Address Architecture for Parallel, Dynamically Applicant: Michael Baxter Page 13 of 29 S/N 09/255,499 Pocket No.: 20412-02553

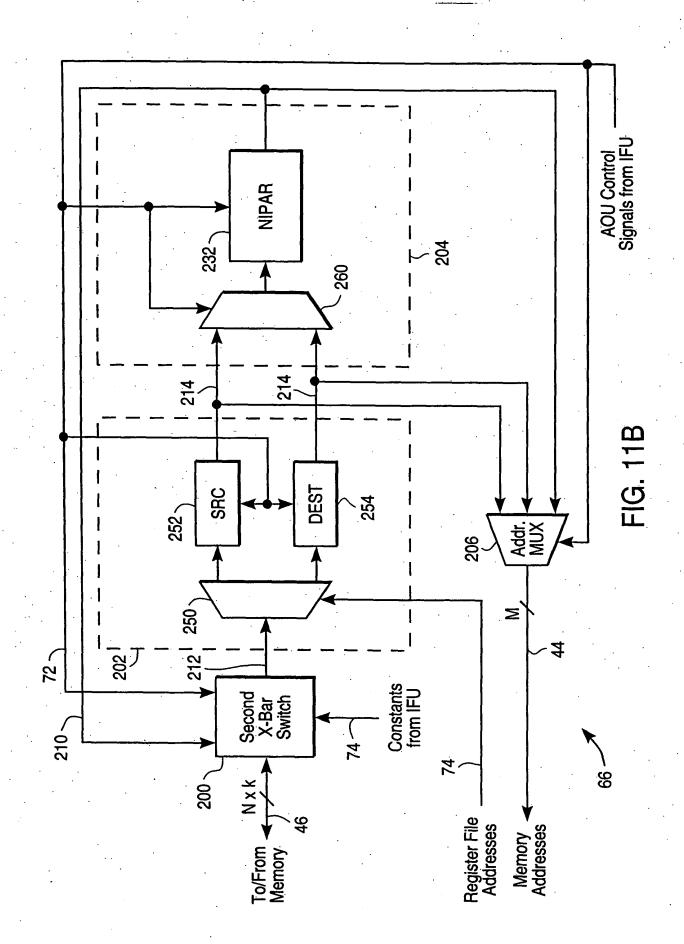


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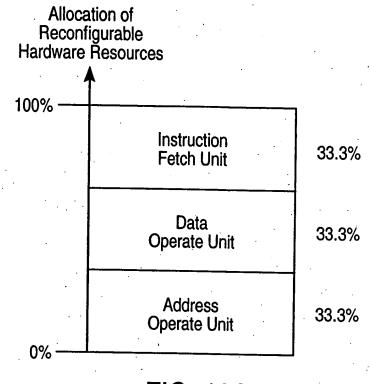


FIG. 12A

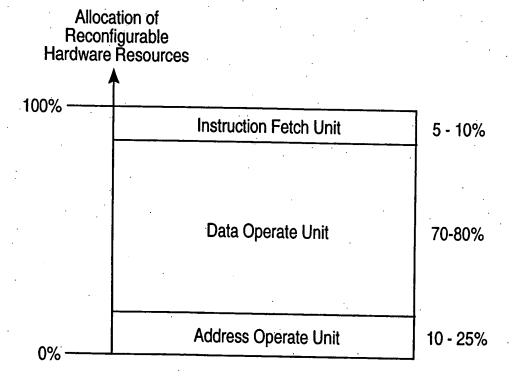
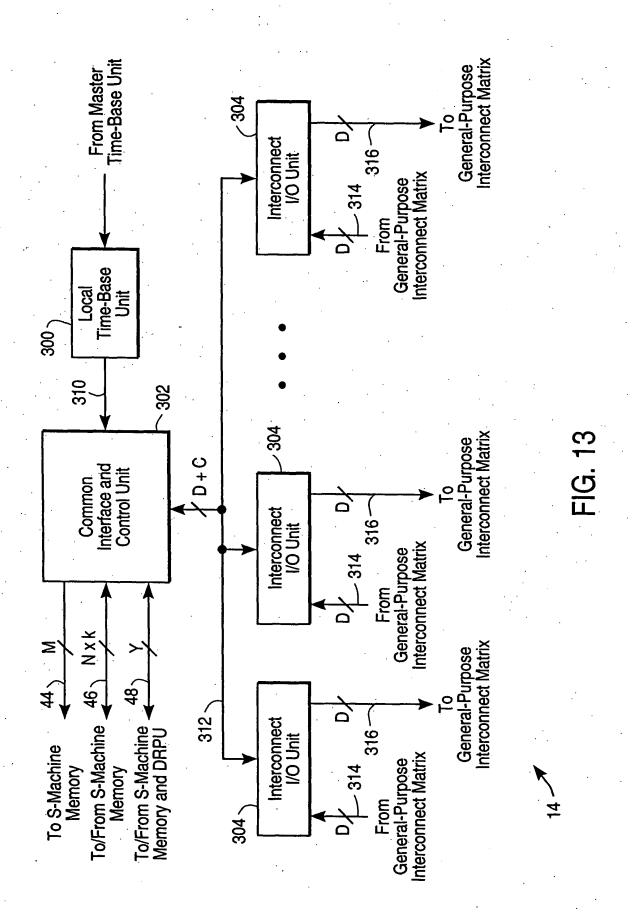


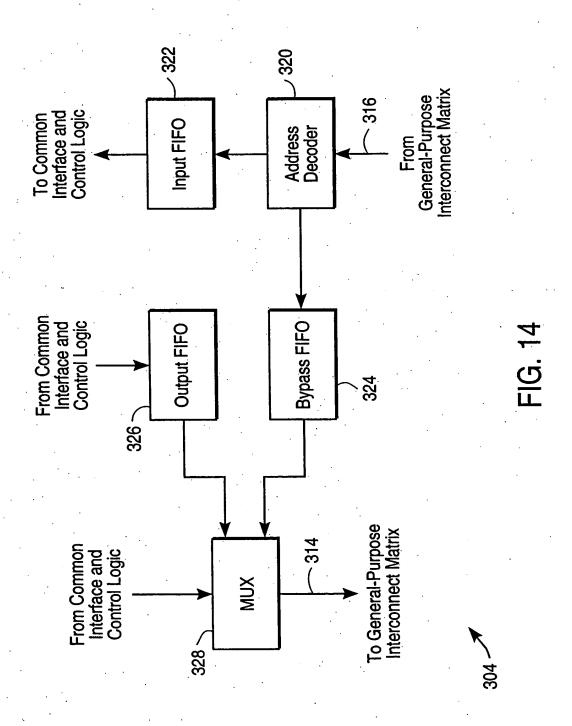
FIG. 12B

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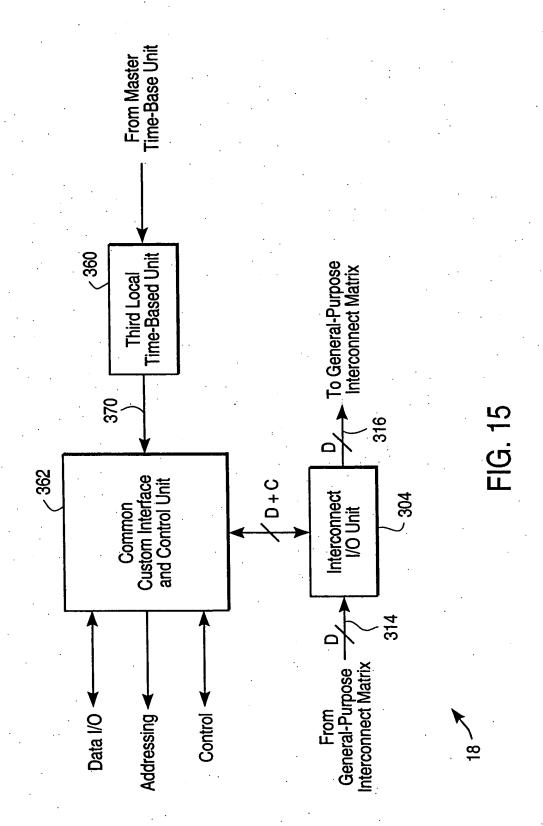
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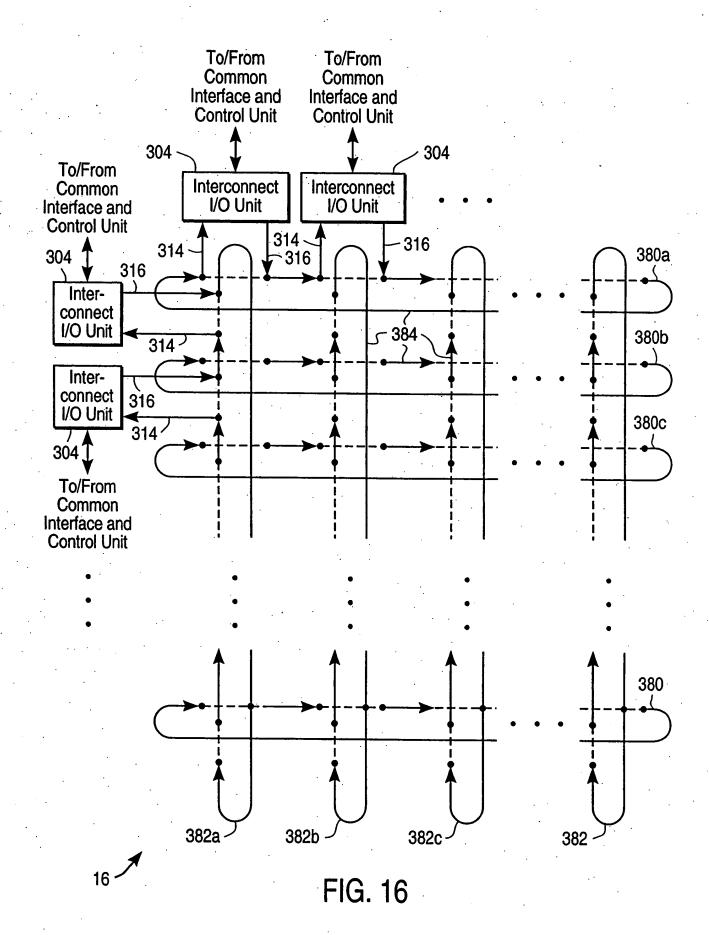
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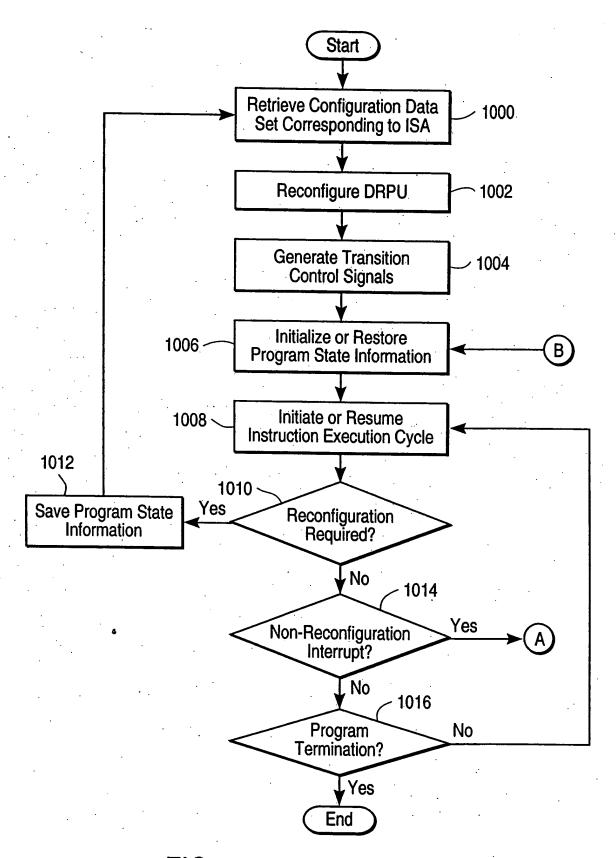


FIG. 17A

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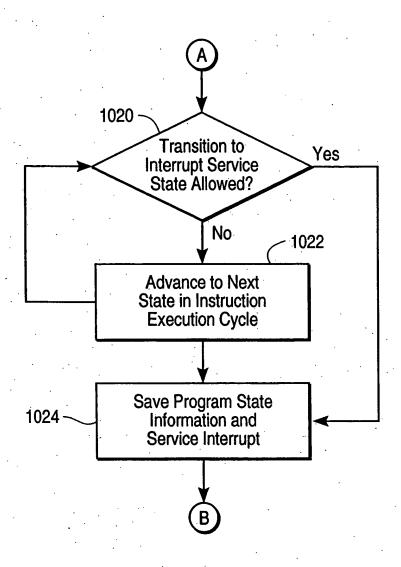
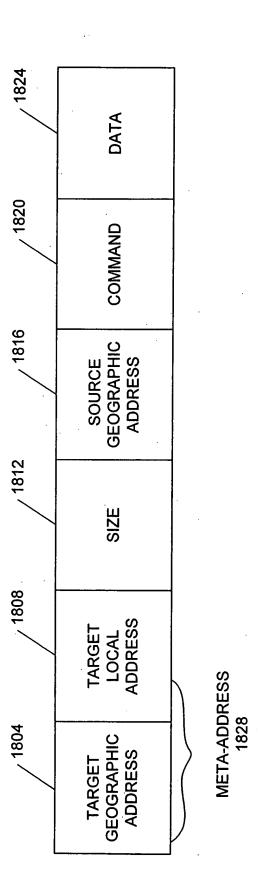


FIG. 17B

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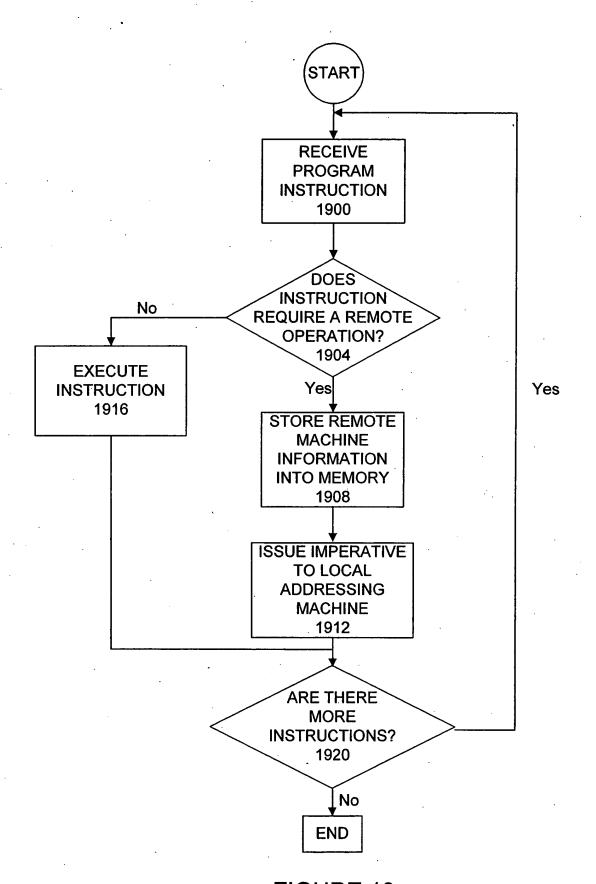


FIGURE 19

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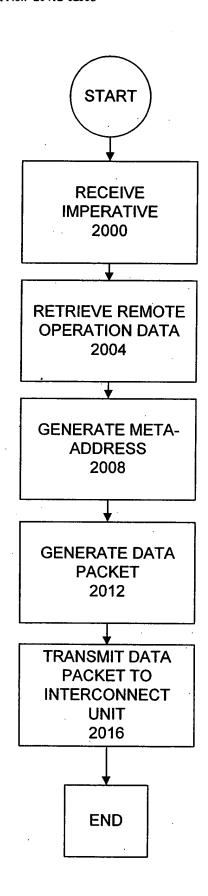
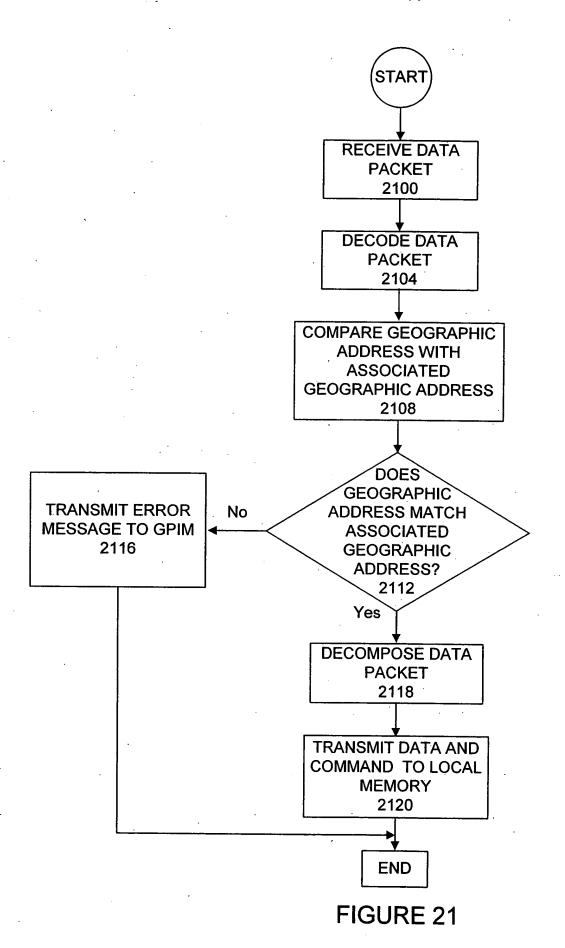


FIGURE 20

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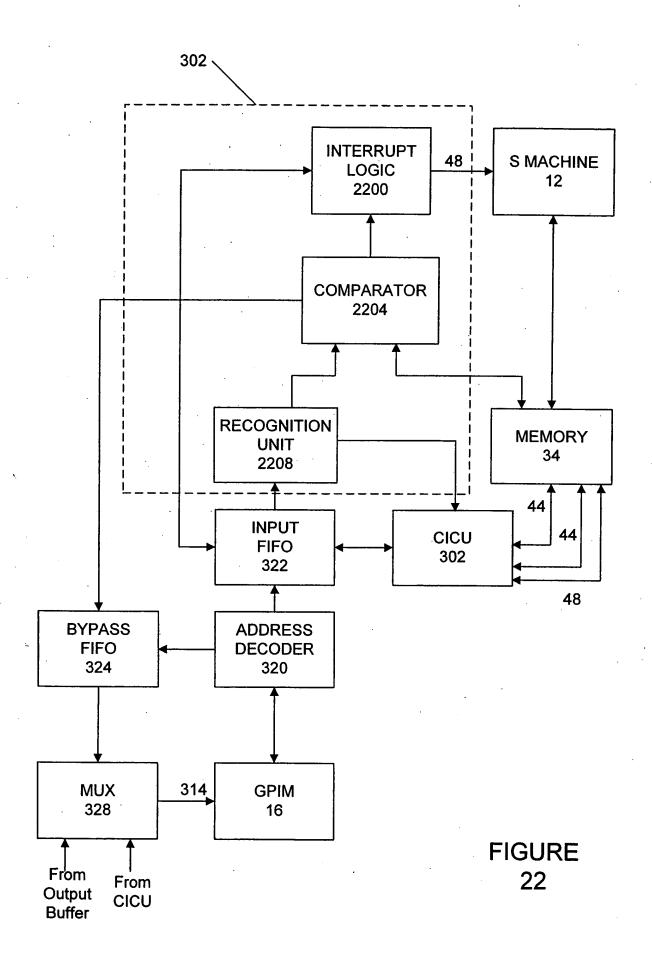
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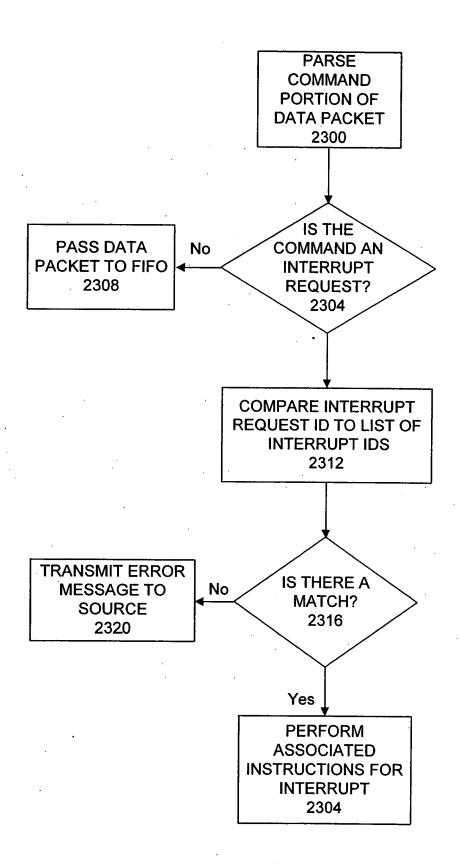


FIGURE 23